Notice of Allowability	Application No.	Applicant(s)	
	10/780,140	DOUGHERTY ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *to the remarks filed on 1/14/08 and interview on 1/18/08*.

2. ☒ The allowed claim(s) is/are *1-3 and 5-20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date same as this notice
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

PAUL DINH
PRIMARY EXAMINER

Paul Dinh

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Robert J. Newman (Reg. No. 60718) on 1/18/08.

The application has been amended as follows:

In the Abstract

The abstract is re-arranged as the following to make the abstract a single paragraph in stead of 2 paragraphs:

ABSTRACT OF THE DISCLOSURE

- - Routability (or wiring congestion) in a VLSI chip is becoming increasingly important as chip complexity increases. Congestion has a significant impact on performance, yield, and chip area. The present invention targets the optimization of congestion early in technology independent synthesis prior to physical design. Instead of attempting to optimize the logic structure as well as the spatial placement of a circuit, we pose a more modest goal limiting such optimization to the scope of logic synthesis. That is, we propose an aggressive optimization approach that is cognizant of circuit structure during technology independent synthesis and produces more predictable implementations which give better routability and yield. - -

(*Note that the text in the abstract remains original*)

In the claims

a. Cancel claim 4.

b. In claim 1, line 13, after the words "metric during", insert - - a technology independent synthesis stage of - -.

c. In claim 13, line 14, after the words "metric during", insert - - a technology independent synthesis stage of - -.

d. In claim 14, line 6, after the words "metric during", insert - - a technology independent synthesis stage of - -.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance:

Claims 1-3 and 5-20 are allowed because the prior art does not teach or suggest a method/program/system for designing/optimizing circuits/circuit design model in the manner as recited in the claims, the method/program/system having the following features in claim 1 and similar recited independent claims 13-14:

Performing logical synthesis using the RTL textual description, the logical synthesis being performed before assigning physical locations to the circuits, wherein performing logical synthesis comprises:

Generating a logic network from the RTL textual description of the circuit design model;

Determining a structural metric through an analysis of the logic network, wherein the structural metric is a measure of wiring congestion of the circuit design model; and

Using the structural metric during a technology independent synthesis stage of the logical synthesis to predict wiring congestion of the circuit design model to optimize the circuit design model.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL DINH whose telephone number is 571-272-1890. If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Jack Chiang can be reached on 571-272-7483. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul Dinh
Primary Examiner